AGC

Your Dreams, Our Challenge

TACONIC

*fast*Rise™ TC/HF for Indestructible Stacked Microvias

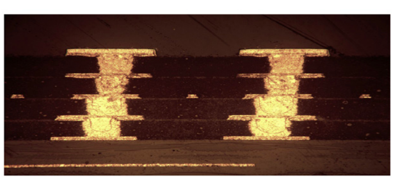
*fast*Rise™ TC/HF are free standing, non-reinforced resin systems designed with extremely low X, Y, Z thermal expansion. *fast*Rise TC is a higher DK, non-flame retardant build-up film. *fast*Rise HF is a 94 V0, conventionally flame retarded, brominated non-reinforced build-up film. *fast*Rise TC/HF have coefficients of thermal expansion from 16 ~ 22 ppm/°C over the temperature range from 30°C to 260°C. Both build-up films are close to the thermal expansion rates of copper (18 ppm/°C) and aluminum (24 ppm/°C) to minimize any stress that occurs during temperature excursions caused by the mismatched expansion rates of the metal and the dielectric material. *fast*Rise TC/HF were designed to meet the current and future needs of:

1. High density (HDI) laser formed interconnects
2. Applications requiring critical thermal reliability such as space and avionics
3. Applications in need of thermal conductivity to spread heat away from hot spots

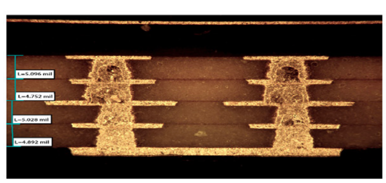
Both *fast*Rise TC and *fast*Rise HF have low dissipation values and are suitable for both high frequency microwave and digital electronics. To achieve high thermal stability, the following characteristics are important:

1. Low thermal expansion and contraction above and below T_g
2. A high T_g (>225°C) or non-observable T_g to minimize any expansion from room temperature to 260°C
3. Low modulus

Materials can have very low CTE values and be very brittle and prone to cracking. The ideal material has a low modulus, is conformable, and is capable of some amount of elongation and does not crack. *fast*Rise TC has been designed for low CTE, high T_g, and as low a modulus as possible and still retain other key properties.



Scan shows 4 stacks of microvias and the adjoining finely etched traces.



Scan shows consistent layer to layer thickness after each sequential lamination.

Benefits & Applications:

- Passes 200 reflow cycles 35-260 °C
- Low thermal expansion closely matched to copper and aluminum
- Low modulus, surface conformal layer to prevent pad cratering
- High 0.94 W/M*K thermal conductivity for *fast*Rise™ TC
- Capable of simultaneously bonding subassemblies together and via filling
- High flow and fill for sequential lamination and filling heavy 4 oz copper layers
- Solves problems with polyimide cracks. Excellent bonding material to cores for heavy copper/high power applications
- Leveling agent properties leaving very flat surfaces for large semiconductor attach

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- Semiconductor pin routing (HDI)
- Power Amplifiers
- Aviation
- Space
- Military

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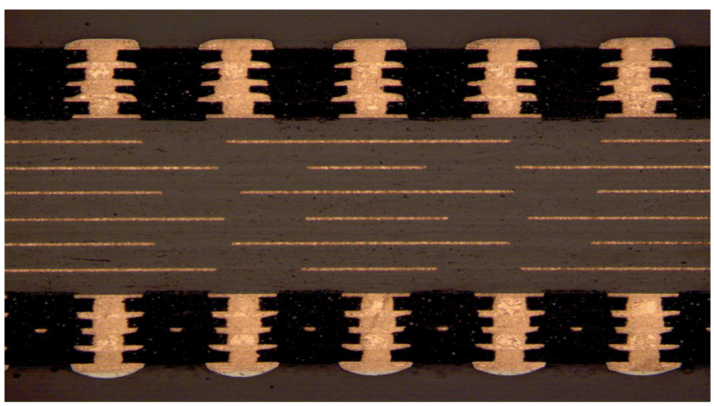
*fast*Rise™ TC/HF for Indestructible Stacked Microvias

High Density Interconnects pose many material challenges. f*ast*Rise buildup films address these challenges with the following features:

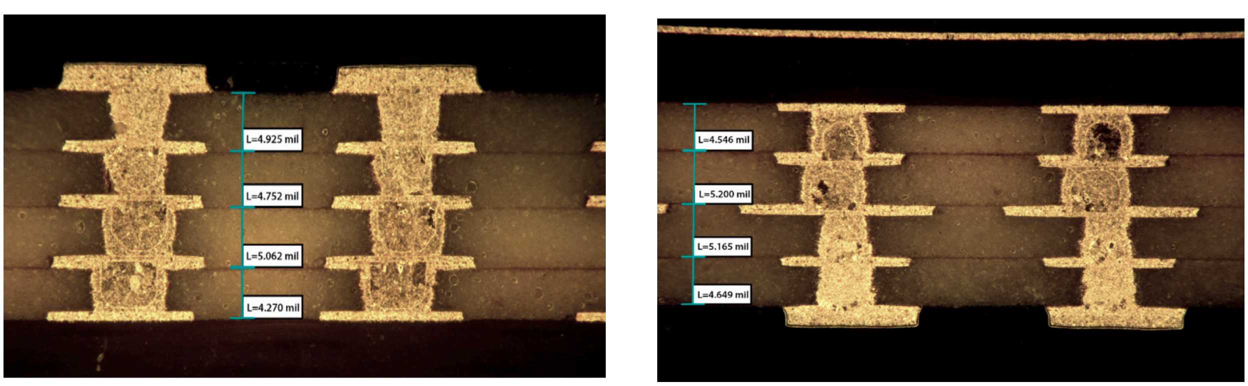
1. High flow and fill to encapsulate circuitry between sequential laminations to avoid any chemical infiltration.
2. Enough flow with 1 ply of bonding material.
3. Sufficient copper adhesion to survive all PWB fabrication steps including planarization and routing.
4. Good lasability for via formation and a wide enough process window to account for varying thickness as a result of uneven copper distribution.
5. Temperature stability through many sequential laminations.

f*ast*Rise TC acts as a leveling agent and will level off thickness variations in a subassembly. It is important that a subassembly be as flat as possible to achieve a uniform dielectric thickness of *fast*Rise TC during the first foil lamination. *fast*Rise TC is available in 1.2 to 2.5 mil in thickness, laser drills readily with a large process window and overcomes wide thickness variations from an underlying subassembly. f*ast*Rise buildup films have shown exceptional performance with either D Coupon reflow testing or CITC coupon testing.

*fast*Rise TC passes 200 cycles 35 – 260° C of reflow with layers of 4 stacked microvias.



*fast*Rise TC D-coupon top to bottom

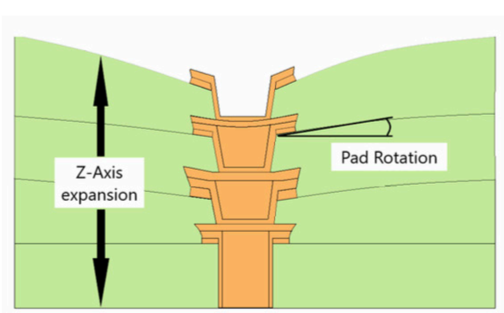


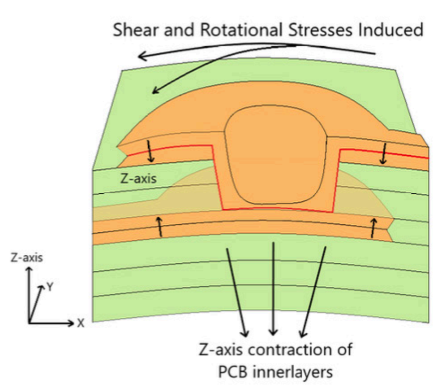
These two graphs show the respective dielectric thicknesses layer to layer when looking at the top and bottom of the FR4 subassembly.

*fast*Rise™ TC Typical Values

Property	Test Method	Unit	Value	Unit	Value
Available Thickness		mil	1.2 / 2.5	mil	1.2 / 2.5
Dk @ 10 GHz	IPC-650 2.5.5.5.1 (modified)		4.8		4.8
Df @ 10 GHz	IPC-650 2.5.5.5.1 (modified)		0.0023		0.0023
Dielectric Breakdown @20 mil	ASTM D 149	kV	18.3	kV	18.3
Dielectric Strength	ASTM D 149	V/mil	808	Kv/mm	31.81
Moisture Absorption	IPC-TM 650-2.6.2.1	%	0.0704	%	0.0704
Flexural Strength (MD)	ASTM 790	psi	3,600	N/mm^2	25
Flexural Strength (CD)	ASTM 790	psi	3,770	N/mm^2	26
Flexural Modulus (MD)	ASTM 790	psi	145,000	N/mm^2	1,000
Flexural Modulus (CD)	ASTM 790	psi	132,000	N/mm^2	910
Tensile Strength (MD)	IPC-650 2.4.18.3	psi	1,595	N/mm^2	11
Tensile Strength (CD)	IPC-650 2.4.18.3	psi	1,595	N/mm^2	11
Elongation at Break (MD)	IPC-650 2.4.18.3	%	9.7	%	9.7
Elongation at Break (CD)	IPC-650 2.4.18.3	%	12	%	12
Young’s Modulus (MD)	IPC-650 2.4.18.3	psi	107,000	N/mm^2	738
Young's Modulus (CD)	IPC-650 2.4.18.3	psi	118,000	N/mm^2	814
Poisson's Ratio	ASTM D638		0.212		0.212
Peel Strength (After Solder Float)	IPC-650 2.4.9E	lbs/in	3.5	N/mm	0.61
Thermal Conductivity	IPC-650 2.4.50	W/M*K	0.94	W/M*K	0.94
Dimensional Stability (MD) – After Press	IPC-650 2.2.4 (TS)	mils/in	-0.049	mm/M	-0.049
Dimensional Stability (CD) – After Press	IPC-650 2.2.4 (TS)	mils/in	0.131	mm/M	0.131
T_g	IPC-650 2.4.41/TMA	°F	437	°C	225
Surface Resistivity	IPC-650 2.5.17E	Mohm/cm	$7.4x10^8$	Mohm/cm	$7.4x10^8$
Volume Resistivity	IPC-650 2.5.17E	Mohm	$1.8x10^8$	Mohm	$1.8x10^8$
CTE - X (RT to 260°C)	IPC-650 2.4.41/TMA	ppm/°C	22	ppm/°C	22
CTE - Y (RT to 260°C)	IPC-650 2.4.41/TMA	ppm/°C	22	ppm/°C	22
CTE - Z (RT to 260°C)	IPC-650 2.4.41/TMA	ppm/°C	22	ppm/°C	22
Density	IPC-650 2.3.5	g/cm^3	2.22	g/cm^3	2.22
T_d (2% Wt. Loss)	IPC-650 2.4.24.6 (TGA)	°F	675	°C	357
T_d (5% Wt. Loss)	IPC-650 2.4.24.6 (TGA)	°F	756	°C	402

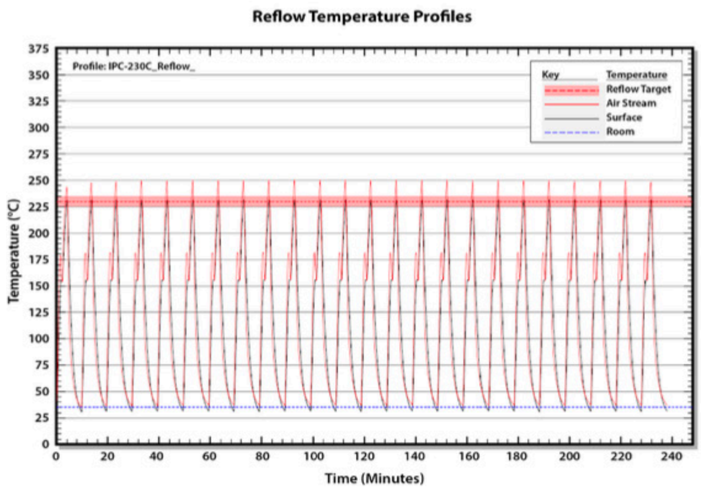
All reported values are typical and should not be used for specification purposes. In all instances, the user shall determine suitability in any given application.



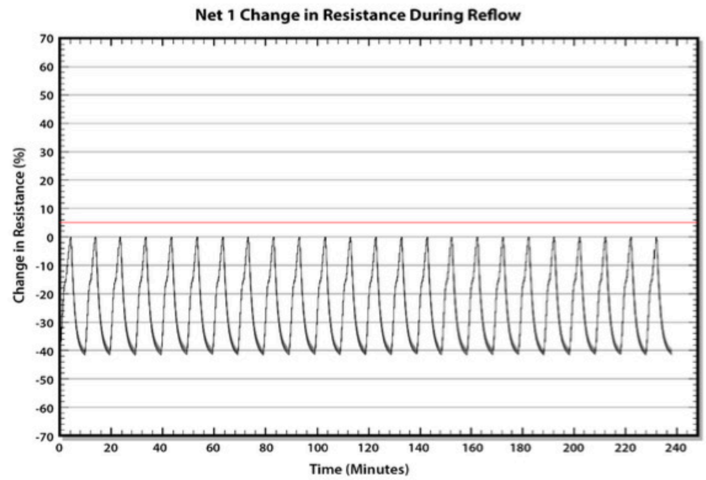


Separation occurs at the onset of cooling ~ 190°C

*fast*Rise™ TC/HF for Indestructible Stacked Microvias



A



B

24 TTM produced D-coupons passed 24 cycles 35 - 260 °C. The 24 coupons were divided: 8 coupons were solder floated at 270 °C, 8 coupons at 280 °C, and 8 coupons at 288 °C. The 24 D-coupons were then thermocycled another 24 times at Robisan Labs. All 24 coupons passed 48 cycles 35 - 260 °C with all of them being solder floated from 270 - 288 °C. Separately, an experiment was done at TTM thermocycling other coupons to 260 °C. The coupons passed 200 cycles 35 - 260 °C.

Reflow Statistics

Coupon Number	Nominal Resistance at Room Temperature (ohms)		Reference Resistance at 230C (ohms)		Cycles to 5% Change		Change after 24 Cycles (%)	
	Net 1 - Lot #1	Net 1 - Lot #2	Net 1 - Lot #1	Net 1 - Lot #2	Net 1 - Lot #1	Net 1 - Lot #2	Net 1 - Lot #1	Net 1 - Lot #2
1	0.981	0.943	1.621	1.581	>24	>24	-0.1	-0.4
2	0.952	0.987	1.599	1.693	>24	>24	0.0	-0.3
3	0.916	0.983	1.554	1.671	>24	>24	-0.0	0.2
4	0.893	0.972	1.509	1.655	>24	>24	-0.1	0.0
5	0.908	0.978	1.538	1.671	>24	>24	0.2	0.1
6	0.910	0.959	1.530	1.615	>24	>24	0.1	-0.0
7	0.899	0.936	1.511	1.561	>24	>24	0.1	-0.1
8	0.911	0.995	1.560	1.685	>24	>24	-0.1	-0.2
9	0.942	0.940	1.601	1.601	>24	>24	-0.1	-0.2
10	0.913	0.961	1.571	1.635	>24	>24	-0.1	-0.2
11	0.911	0.927	1.587	1.569	>24	>24	-0.1	-0.1
12	0.891	0.949	1.542	1.593	>24	>24	-0.2	-0.2
13	0.895	0.920	1.538	1.565	>24	>24	-0.2	-0.2
14	0.911	0.936	1.581	1.614	>24	>24	-0.3	-0.2
15	0.883	0.965	1.518	1.661	>24	>24	0.0	-0.2
16	0.910	0.918	1.567	1.588	>24	>24	-0.1	-0.4
17	0.887	0.903	1.532	1.564	>24	>24	-0.0	-0.2
18	0.904	0.909	1.551	1.554	>24	>24	-0.1	-0.4
19	0.908	0.934	1.545	1.598	>24	>24	-0.1	-0.2
20	0.905	0.922	1.546	1.592	>24	>24	0.1	-0.1
21	0.899	0.925	1.531	1.598	>24	>24	-0.1	-0.1
22	0.901	0.888	1.523	1.528	>24	>24	-0.0	-0.1
23	0.899	0.939	1.523	1.617	>24	>24	0.1	-0.1
24	0.896	0.975	1.487	1.687	>24	>24	0.1	0.1

*fast*Rise™ HF Typical Values (FR-HF-0015, FR-HF-0025)					
Property	Test Method	Unit	Value	Unit	Value
Available Thickness		mil	1.37/2.5	microns	34/62.5
Dk @10 GHz (SPC)	IPC-650 2.5.5.13 (modified)		3.23		3.23
Df @10 GHz (SPC)	IPC-650 2.5.5.13 (modified)		0.0019		0.0019
Dk @10 GHz (Bereskin)	IPC 2.5.5.1		3.17		3.17
Dielectric Breakdown @20 mils	ASTM D 149	kV	16.7	kV	16.7
Dielectric Strength	ASTM D 149	V/mil	835.7	Kv/mm	32.9
Moisture Absorption	IPC-650-2.6.2.1	%	0.3	%	0.3
Flexural Strength	ASTM 790	kpsi	9.35	N/mm²	64.5
Flexural Modulus	ASTM 790	kpsi	923	N/mm²	6425
Tensile Strength	IPC-650 2.4.18.3	kpsi	4.93	N/mm²	34
Tensile Modulus	IPC-650 2.4.18.3	kpsi	1494	N/mm²	10,300
Elongation at Break	IPC-650 2.4.18.3	%	0.4	%	0.4
Poisson's Ratio			0.3		0.3
Peel Strength	IPC-650 2.4.9E	lbs/in	3.0 - 4.0	N/mm	
Resin Flow		%	40	%	40
Thermal Conductivity	IPC-650 2.4.50	W/M*K		W/M*K	
Dimensional Stability (MD) – After Press	IPC-650 2.2.4 (TS)	mils/in		mm/M	
Dimensional Stability (CD) – After Press	IPC-650 2.2.4 (TS)	mils/in		mm/M	
T_g	IPC-650 2.4.41/DSC	°F	255, 520	°C	124, 271
T_g	IPC-650 2.4.41/TMA	°F	262, 529	°C	128, 276
T_g	IPC-650 2.4.25/DMA	°F	363, 502	°C	184, 261
Surface Resistivity	IPC-650 2.5.17E	Mohm	1.83E+15	Mohm	1.83E+15
Volume Resistivity	IPC-650 2.5.17E	Mohm/cm	6.48E+15	Mohm/cm	6.48E+15
CTE (40° to 260°C)	IPC-650 2.4.41/TMA	ppm/°C	30.6	ppm/°C	30.6
CTE (40° to 260°C)	IPC-650 2.4.41/TMA	%	0.67	%	0.67
Density	IPC-650 2.3.5	g/cm³	1.7	g/cm³	1.7
Flammability*	94 V0		Pass		Pass
T_d (2% Wt. Loss)	IPC-650 2.4.24.6 (TGA)	°F	696	°C	369
T_d (5% Wt. Loss)	IPC-650 2.4.24.6 (TGA)	°F	748	°C	398
T-288	IPC-650 2.4.24.6 (TGA)	°F	120+ min	°C	120+ min
T-300	IPC-650 2.4.24.6 (TGA)	°F	120+ min	°C	120+ min

*Organic phosphorous flame retardant
ND = Not Detectable

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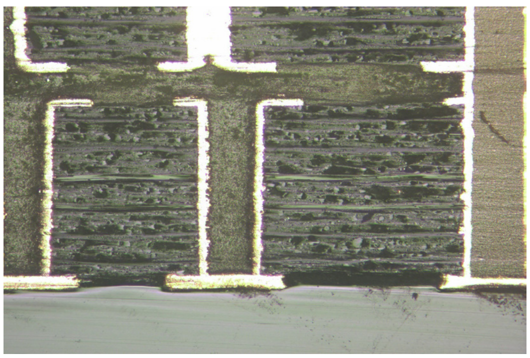
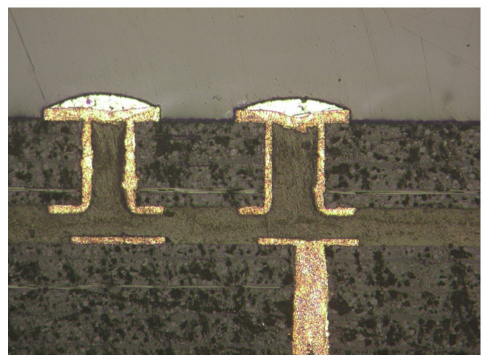
Simultaneous Bonding of Multilayer Subassemblies

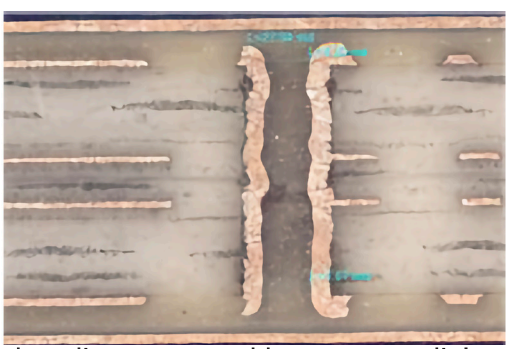
The non-reinforced series of f*ast*Rise is well suited to the simultaneous bonding of subassemblies and via filling. f*ast*Rise EZpure/TC/HF all have extremely high IPC flow values, reach low viscosities, flow with low pressure and fill thousands of ground vias with no voiding. Holding multilayer registration via filling thin subassemblies can be problematic due to core distortion caused by planarization. Planarization causes less misregistration when it is conducted on a much thicker subassembly formed by the simultaneous via filling and bonding of thin subassemblies. The following costs can be removed by the simultaneous bonding and via filling of two subassemblies: resist coating/imaging, button plating, resist strip, via fill, epoxy cure, planarization. Epoxy via fill materials have limitations such as solvent outgassing, moisture uptake, high CTE values not matched to copper. Copper pastes are prone to voids.



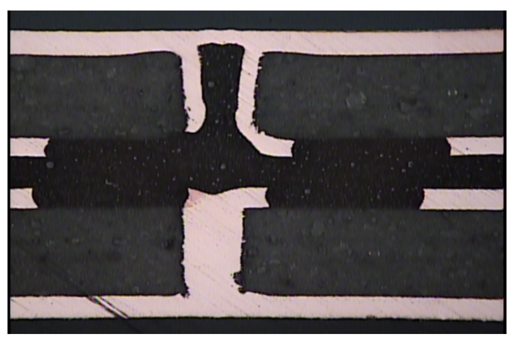
f*ast*Rise simultaneously bonding together two subassemblies and filling 10,000 30 mil deep ground vias (side 1).



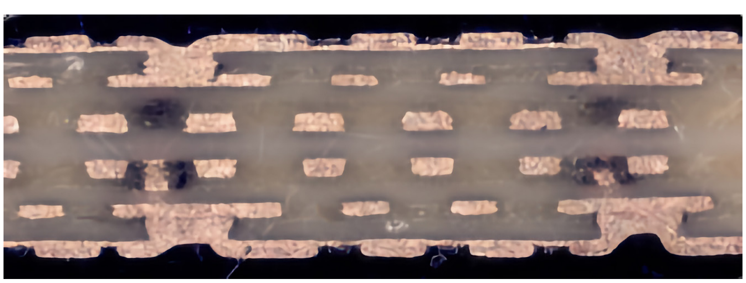
f*ast*Rise simultaneously bonding together two subassemblies and filling 10,000 10 mil deep ground vias (side 2).



f*ast*Rise bonding a top and bottom cap dielectric layer and simultaneously via filling 13K buried vias, 28 mil deep.



f*ast*Rise TC simultaneously bonding together a subassembly and via filling.



One advantage of the f*ast*Rise build up family of products is that they act as leveling agents. Very flat surfaces can be obtained and this is a large benefit when attaching large semiconductors.